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UNITED STATES PATENT APPLICATION

CONTACT STRUCTURE

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CONTACT STRUCTURE

Field of the Invention

This invention relates to contact structures, and more particularly to contact structures used in the fabrication of integrated circuits.

Background of the Invention

An integrated circuit, such as a dynamic random access memory (DRAM) includes passive devices, such as capacitors, and active devices, such as metal-oxide semiconductor field-effect transistors (MOSFETS), fabricated on a single substrate. In fabricating an integrated circuit to perform a particular function, the passive and active devices are coupled together. For example, a capacitor electrode is electrically coupled to a MOSFET drain or source to form a dynamic random access memory (DRAM) cell for storing information.

One method of coupling a capacitor electrode to a MOSFET drain or source includes the operation of directly coupling the capacitor electrode to the drain or source by fabricating the capacitor electrode at the drain or source. Unfortunately, several problems arise when a non-silicon electrode is directly coupled to a MOSFET drain or source. First, the electrode can experience oxidation, which interferes with the electrode conductivity and may cause unpredictable memory cell operation. Electrode oxidation is most likely to occur during capacitor formation processes performed in an O_2 atmosphere. Second, atomic migration to and from a substrate, such as silicon substrate, may occur between the substrate in which the MOSFET source and drain are formed and other integrated circuit elements, such as the dielectric layer of a capacitor. Atomic migration alters the electrical properties of the integrated circuit elements and may cause unpredictable memory cell operation.

One solution to these problems is to form a contact structure having a barrier layer located between the electrode and the source or drain for blocking oxygen migration and atomic migration to and from the substrate. Unfortunately, a single barrier layer that effectively blocks both oxygen migration and atomic migration from the substrate may

react with the conductive layer fabricated at the source or drain and cause unpredictable circuit operation.

For these and other reasons, there is a need for the present invention.

Summary of the Invention

The above mentioned problems with coupling devices in integrated circuits and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A contact structure is described that includes one or more layers and other structures for blocking atomic migration in an integrated circuit, which improves the reliability of the circuit.

The present invention provides, in one embodiment, a contact including a polysilicon layer formed on a substrate, one or more barrier layers formed above the polysilicon layer, and a barrier structure encircling the polysilicon layer and the one or more barrier layers. The polysilicon layer provides a conductive material for coupling to an active or a passive device in an integrated circuit. At least one of the one or more barrier layers restricts the migration of atoms to and from the substrate, and at least one of the one or more barrier layers restricts the migration of oxygen atoms. Restricting the migration of substrate atoms, prevents the electrical properties of the integrated circuit devices from being inadvertently altered during circuit fabrication. Restricting the migration of oxygen atoms, deters oxidation at electrode surfaces, such as capacitor electrode surfaces. Since the barrier layers of the contact are also electrically conductive, the contact is suitable for use in interconnecting integrated circuit devices.

In an alternate embodiment, the present invention provides a method of fabricating a contact. The method includes forming a polysilicon layer and a tungsten nitride layer above a base integrated circuit structure. The polysilicon layer is formed at an electrical connection site of an integrated circuit device. The polysilicon layer and the tungsten nitride layer are etched to a level below the surface of the base integrated circuit structure. The polysilicon layer encircling the contact is etched much deeper, and a silicon nitride layer is formed to encircle the tungsten nitride layer. A ruthenium silicide layer is formed above the tungsten nitride layer as an oxygen barrier. The silicon nitride

layer prevents the polysilicon layer from reacting with the ruthenium silicide layer. After polishing and cleaning, the ruthenium silicide layer is ready for coupling to an integrated circuit device.

Brief Description of the Drawings

Figure 1 is an illustration of a cross-sectional view of one embodiment of a contact structure.

Figure 2 is an illustration of a cross-sectional view of one embodiment of an integrated circuit structure suitable for use as a foundation for a contact structure.

Figure 3 is an illustration of a cross-sectional view of one embodiment of a partially formed contact structure.

Figure 4 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure of Figure 3 after etching.

Figure 5 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure of Figure 4 after the formation of a barrier structure and a second barrier layer.

Figure 6 is an illustration of a cross-sectional view of one embodiment of the contact structure of Figure 5 after cleaning and polishing.

Figure 7 is an illustration of a cross-sectional view of an alternate embodiment of a contact structure.

Figure 8 is an illustration of a cross-sectional view of one embodiment of a partially formed contact structure.

Figure 9 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure of Figure 8 after chemical mechanical polishing (CMP).

Figure 10 is an illustration of a cross-sectional view of one embodiment of the partially formed contact of Figure 9 after etching.

Figure 11 is an illustration of a cross-sectional view of one embodiment of the partially formed contact of Figure 10 after depositing an oxide layer.

Figure 12 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure of Figure 11 after etching the oxide layer.

Figure 13 a block diagram of a computer system suitable for use in connection with the present invention.

Detailed Description

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 1 is an illustration of one embodiment of contact structure 100 coupling device 103 to device 105 in integrated circuit 107. Contact structure 100 provides a conductive path for transmitting an electrical signal between devices 103 and 105. Contact structure 100, in one embodiment, includes polysilicon layer 109, barrier layers 111 and 113, and barrier structure 115. Devices 103 and 105, which are coupled together by contact structure 100, are not limited to a particular type of device. Devices 103 and 105 may be any type of active or passive device capable of being fabricated using integrated circuit technologies, such as metal-oxide semiconductor (MOS) or bipolar technologies. In the example embodiment shown in Figure 1, device 103 is a capacitor and device 105 is a metal-oxide semiconductor field effect transistor (MOSFET). However, contact structure 100 is not limited to use in connection with a particular type of integrated circuit 107. Contact structure 100 is suitable for use in connection with linear integrated circuits, such as operational amplifiers, digital integrated circuits, such as boolean logic circuits and storage circuits, and memory circuits, such as dynamic random access memory (DRAM) circuits, static random access memory (SRAM) circuits, erasable programmable read only memory (EPROM) circuits, electrically

erasable programmable read only memory (EEPROM) circuits, and flash memory circuits.

A structure described herein encircles a second structure or layer when the structure partially or completely surrounds any portion of the second structure or layer. For example, in Figure 1 barrier structure 115 encircles polysilicon layer 109 and barrier layers 111 and 113.

Figures 2-7 illustrate a series of cross-sectional views of integrated circuit 107 during the fabrication of contact structure 100. Figure 2 illustrates one embodiment of base structure 201 suitable for use as a foundation for the fabrication of contact structure 100. Base structure 201 includes substrate 117, circuit structures 203 and 204 including polysilicon layer 205 and silicon nitride layer 207, and borophosphosilicate glass (BPSG) layer 209. BPSG layer 209 is etched to form plug volume 211.

Substrate 117 is preferably fabricated from a material, such as a semiconductor, that is suitable for use as a substrate in connection with the fabrication of integrated circuits. Substrate 117 includes doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures having an exposed surface with which to form the contact structures of the present invention. Substrate 117 refers to semiconductor structures during processing, and may include other layers that have been fabricated thereon. In one embodiment, substrate 117 is fabricated from silicon. Alternatively, substrate 117 is fabricated from germanium, gallium-arsenide, silicon-on-insulator, silicon-on-sapphire, or any other crystalline or amorphous material suitable for use as a substrate in the manufacture of integrated circuits. Substrate 117 is not limited to a particular material, and the material chosen for the fabrication of substrate 117 is not critical to the practice of the present invention.

Figure 3 is an illustration of a cross-sectional view of one embodiment of a partially formed contact structure 100 including polysilicon layer 109 and barrier layer 111. Polysilicon layer 109 is deposited above base structure 201 to a thickness of between about 450 angstroms and 550 angstroms. The thickness of polysilicon layer 109 is not critical to the performance of the present invention, and the thickness of polysilicon

layer 109 may be varied to meet the design rules of a particular integrated circuit fabrication process. After polysilicon layer 109 is deposited, barrier layer 111 is deposited above polysilicon layer 109. Barrier layer 111 prevents the diffusion of substrate atoms beyond barrier layer 111 and provides a conductive path between device 103 and device 105, as shown in Figure 1. In one embodiment, barrier layer 111 is fabricated from tungsten nitride and has a thickness of between about 900 angstroms and 1100 angstroms. A thickness of less than about 900 angstroms does not sufficiently block the etch during the removal of the encircling polysilicon. A thickness of more than about 1100 angstroms causes contact structure 100 to have very little space remaining for the ruthenium silicide. During the formation of barrier layer 111, voids may form in the layer. Although it is preferable to avoid the formation of voids in barrier layer 111, the operation of contact structure 100 is not significantly degraded by the formation of voids.

Figure 4 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure, which is shown in Figure 3, after etching. Barrier layer 111 and polysilicon layer 109 are etched to a level below the surface of the BPSG layer 209. Polysilicon layer 109 is preferably etched long enough to recess the outer perimeter of the plug volume 211 down to circuit structures 203 and 204.

Figure 5 is an illustration of one embodiment of the partially formed contact structure shown in Figure 4 after the formation of barrier structure 115 and barrier layer 113. Barrier structure 115 prevents polysilicon layer 109 from interacting with barrier layer 113. In one embodiment, barrier structure 115 is fabricated by forming a layer of silicon nitride above substrate 117 and etching the silicon nitride to a level below the surface of BPSG layer 209. Barrier structure 115 has a thickness that is about equal to the thickness of polysilicon layer 109. After barrier structure 115 is fabricated, barrier layer 113 is fabricated above barrier layer 111 and barrier structure 115. Barrier layer 113 prevents oxygen from diffusing into substrate 117 and provides a conductive path between device 103 and device 105, as shown in Figure 1. In one embodiment, barrier layer 113 is fabricated by forming a layer of platinum-iridium (PtIr) above barrier layer 111 and barrier structure 115. In an alternate embodiment, barrier layer 113 is fabricated

by forming a layer of platinum-rhodium (PtRh) above barrier layer 111 and barrier structure 115.

Figure 6 is an illustration of one embodiment of the contact structure shown in Figure 5 after cleaning and polishing. A chemical-mechanical polishing (CMP) process and a post CMP process is applied contact structure 100 and to the surface of substrate 117. The post CMP process is either a wet or sputter etch for removing CMP residue and smeared barrier material. After the post CMP process, device 103, as shown in Figure 1, may be fabricated above contact structure 100. In one embodiment, device 103 is a capacitor having a pair or electrodes 119 and 121 and a dielectric 123 for storing charged sensed by device 105.

Referring again to Figure 1, in operation, contact structure 100 provides a conductive path for the exchange of electronic signals between devices 103 and 105. For example, in a DRAM cell in which device 103 is a capacitor and device 105 is a MOSFET, contact structure 100 provides a path so that the MOSFET is capable of sensing charge stored on the capacitor. Contact structure 100 also provides a barrier layer 111 for blocking the migration of substrate atoms into the upper layers of integrated circuit 107. In addition, contact structure 100 provides barrier layer 113 for blocking the migration of oxygen atoms into substrate 117.

Figure 7 is an illustration of a cross-sectional view of an alternate embodiment of a contact structure. Contact structure 700 couples device 103 to device 105 in integrated circuit 707. Contact structure 700 provides a conductive path for transmitting an electrical signal between devices 103 and 105. Contact structure 700, in one embodiment, includes polysilicon layer 709, barrier layers 711 and 713, and barrier structure 715. Devices 103 and 105, which are coupled together by contact structure 700, are not limited to a particular type of device. Devices 103 and 105 may be any type of active or passive device capable of being fabricated using integrated circuit technologies, such as metal-oxide semiconductor (MOS) or bipolar technologies. In the example embodiment shown in Figure 7, device 103 is a capacitor and device 105 is a metal-oxide semiconductor field effect transistor (MOSFET). However, contact structure 700 is not limited to use in connection with a particular type of integrated circuit 707. Contact

structure 700 is suitable for use in connection with linear integrated circuits, such as operational amplifiers, digital integrated circuits, such as boolean logic circuits and storage circuits, and memory circuits, such as dynamic random access memory (DRAM) circuits, static random access memory (SRAM) circuits, electrically programmable memory (EPROM) circuits, and electrically erasable programmable memory (EEPROM) circuits.

Figure 8 is an illustration of a cross-sectional view of one embodiment of a partially formed contact structure of Figure 7 after the fabrication of one or more layers. The embodiment illustrated in Figure 8 includes base structure 201 including substrate 117, circuit structures 203 and 204, which include polysilicon layer 205 and silicon nitride layer 207, and borophosphosilicate glass (BPSG) layer 209, which are described above in connection with contact structure 100. Also, as described above in connection with contact structure 100, BPSG layer 209 is etched to form plug volume 211. After the formation of plug volume 211, polysilicon layer 803, tungsten nitride layer 805, and RuSix layer 807 are formed above substrate 117. In one embodiment, the thickness of polysilicon layer 803 is about 500 angstroms, the thickness of tungsten nitride layer 805 is about 500 angstroms, and the thickness of RuSix layer 807 is about 2000 angstroms.

Figure 9 is an illustration of a cross-sectional view of one embodiment of the partially formed contact structure of Figure 8 after chemical mechanical polishing (CMP). In performing the CMP it is not necessary to completely remove polysilicon layer 803 from the surface of the BPSG layer 209. The CMP is followed by a dry etch to remove polysilicon layer 803 and tungsten nitride layer 805.

Figure 10 is an illustration of a cross-sectional view of one embodiment of the partially formed contact of Figure 9 after etching. A dry etch removes polysilicon layer 803 from the surface of BPSG 209, and etches polysilicon layer 803 and tungsten nitride layer 805 to a level below the surface of the BPSG layer 209. A dry etch of polysilicon layer 803 removes the polysilicon layer to a level near the surface of circuit structure 203. The dry etch also etches tungsten nitride layer 805 to a level below the surface of BPSG layer 209. Preferably, polysilicon layer 803 is etched to a level below the level of tungsten nitride layer 805.

Figure 11 is an illustration of a cross-sectional view of one embodiment of the partially formed contact of Figure 10 after forming oxide layer 1101. After contact structure 700 is etched as shown in Figure 10, oxide layer 1101 is formed above contact structure 700 and at least partially fills the gap formed between tungsten nitride layer 805 and BPSG layer 209. Since oxide layer 1101 is intended to isolate polysilicon layer 803 from RuSix layer 807, oxide layer 1101 need not fill the gap down to the level of polysilicon layer 803.

Figure 12 is an illustration of a cross-sectional view of one embodiment of contact structure 700 of Figure 11 after etching oxide layer 1101. Oxide layer 1001 is etched to expose RuSix layer 807. After exposing RuSix layer 807, contact structure 700 is capable of coupling device 103 to device 105, as illustrated in Figure 7.

Figure 13 a block diagram of a computer system suitable for use in connection with the present invention. System 1300 comprises processor 1305 and memory device 1310, which includes contact structures of one or more of the types described above in conjunction with Figures 1-12. Memory device 1310 comprises memory array 1315, address circuitry 1320, and read circuitry 1330, and is coupled to processor 1305 by address bus 1335, data bus 1340, and control bus 1345. Processor 1305, through address bus 1335, data bus 1340, and control bus 1345 communicates with memory device 1310. In a read operation initiated by processor 1305, address information, data information, and control information are provided to memory device 1310 through busses 1335, 1340, and 1345. This information is decoded by addressing circuitry 1320, including a row decoder and a column decoder, and read circuitry 1330. Successful completion of the read operation results in information from memory array 1315 being communicated to processor 1305 over data bus 1340.

Conclusion

Contact structures and methods of fabricating contact structures have been described. The contact structures include one or more barrier layers and a barrier structure. One of the barrier layers is capable of blocking the migration of substrate atoms. Another of the barrier layers is capable blocking the migration of oxygen atoms.

The barrier structure prevents at least two layers in the contact structure from reacting with each other. The methods of fabricating the contact structure include processes for forming the layers of the contact structure, etching the layers of the contact structure, forming the barrier structure, and polishing the contact structure.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A contact comprising:

a polysilicon layer formed on a substrate;

one or more barrier layers formed above the polysilicon layer; and

a barrier structure encircling the polysilicon layer and the one or more barrier layers.

2. The contact of claim 1, wherein the one or more barrier layers formed above the polysilicon layer is two.

3. The contact of claim 1, wherein the barrier structure is fabricated from tungsten nitride.

4. A contact comprising:

a polysilicon layer formed on a substrate;

a silicon barrier layer formed above the polysilicon layer;

an oxygen barrier layer formed above the silicon barrier layer; and

a barrier structure encircling the polysilicon layer, the silicon barrier layer, and the oxygen barrier layer.

5. The contact of claim 4, wherein the silicon barrier layer has a thickness of between about 900 and 1100 angstroms.

6. The contact of claim 4, wherein the oxygen barrier layer is fabricated from platinum-iridium.

7. A contact comprising:

a polysilicon layer formed above a substrate;

one or more barrier layers formed above the polysilicon layer; and

a silicon nitride barrier structure encircling the polysilicon layer and the one or more barrier layers.

8. The contact of claim 7, wherein at least one of the one or more barrier layers is fabricated from platinum-rhodium.

9. The contact of claim 7, wherein the polysilicon layer has a thickness of between about 450 angstroms and 550 angstroms.

10. A contact comprising:

a polysilicon layer formed on a substrate;

one or more barrier layers formed above the polysilicon layer; and

a barrier structure including an air gap and an oxide encircling the one or more barrier layers.

11. The contact of claim 10, wherein at least one of the one or more barrier layers is ruthenium silicide.

12. The contact of claim 10, wherein the barrier structure is an oxide layer.

13. A contact comprising:

a polysilicon layer formed on a substrate;

a silicon barrier layer formed above the polysilicon layer;

an oxygen barrier layer formed above the silicon barrier layer; and

a barrier structure encircling the silicon barrier layer and the oxygen barrier layer.

14. The contact of claim 13, wherein the silicon barrier layer is tungsten nitride.

15. The contact of claim 13, wherein the oxygen barrier layer is encircled by an air gap.

16. A contact comprising:

a polysilicon layer formed on a substrate;

a tungsten nitride layer formed above the polysilicon layer;

a ruthenium silicide layer formed above the tungsten nitride layer; and

a barrier structure encircling the tungsten nitride layer and the ruthenium silicide layer.

17. The contact of claim 16, wherein the tungsten nitride layer has a thickness of between about 900 angstroms and 1100 angstroms.

18. The contact of claim 16, wherein the polysilicon layer has a thickness of about 500 angstroms.

19. An integrated circuit comprising:

a first device;

a second device;

a contact coupling the first device to the second device; and

an barrier structure encircling the contact.

20. The integrated circuit of claim 19, wherein the first device is a capacitor.

21. The integrated circuit of claim 19, wherein the second device is a transistor.

22. An integrated circuit comprising:

a first device;

a second device;

one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking oxygen atom migration; and

an structure encircling the one or more layers.

23. The integrated circuit of claim 22, wherein the first device is a capacitor.

24. The integrated circuit device of claim 22, wherein the second device is a MOSFET.

25. An integrated circuit comprising:

a first device;

a second device;

one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking silicon atom diffusion; and

a structure encircling at least two of the one or more layers.

26. The integrated circuit of claim 25, wherein the one or more layers is three.

27. The integrated circuit of claim 25, wherein the structure is fabricated from an oxide.

28. An integrated circuit comprising:

a first device;

a second device;

a multilayer contact including ruthenium silicide, the multilayer contact coupling the first device to the second device; and

an oxide ring encircling the ruthenium silicide.

29. The integrated circuit of claim 28, wherein the multilayer contact includes a polysilicon layer.

30. The integrated circuit of claim 29, wherein the polysilicon layer is separated from the oxide ring by an air gap.

31. An integrated circuit comprising:

a first device;

a second device;

one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking oxygen atom migration; and

an oxide ring structure encircling at least two of the one or more layers.

32. The integrated circuit of claim 31, wherein at least one of the one or more layers is fabricated from a tungsten nitride.

33. The integrated circuit of claim 32, wherein the oxide ring structure is in contact with the tungsten nitride.

34. An integrated circuit comprising:

a first device;

a second device;

one or more layers electrically coupling the first device to the second device, at least one of the one or more layers is capable of blocking the diffusion of silicon; and

an oxide ring structure encircling at least one of the one or more layers.

35. The integrated circuit of claim 34, wherein at least one of the one or more layers is ruthenium silicide.

36. The integrated circuit of claim 34, wherein the second device is an active device.

37. A memory cell comprising:

a capacitor;

a transistor;

a contact structure coupling the capacitor to the transistor; and

an insulating structure encircling the contact structure.

38. The memory cell of claim 37, wherein the transistor is a metal-oxide semiconductor field-effect transistor.

39. The memory cell of claim 37, wherein the contact includes one or more layers.

40. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field effect transistor (MOSFET);

a contact structure coupling the capacitor to the MOSFET; and

an insulating structure encircling the contact structure.

41. The memory cell of claim 40, wherein the MOSFET has a source and the contact couples the capacitor to the source.

42. The memory cell of claim 41, wherein the contact includes at least two barrier layers.

43. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field-effect transistor (MOSFET);

a contact structure including a polysilicon layer, a tungsten nitride layer, and a platinum-iridium layer, the contact coupling the capacitor to the MOSFET; and

an insulating structure encircling the contact structure.

44. The memory cell of claim 43, wherein the insulating structure is fabricated from a tungsten nitride.

45. The memory cell of claim 43, wherein the contact structure separates the platinum-iridium layer from the polysilicon layer.

46. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field effect transistor (MOSFET);

a contact structure including a polysilicon layer, a tungsten nitride layer, and a platinum-ruthenium layer, the contact coupling the capacitor to the MOSFET; and

an insulating structure encircling the contact, the insulating layer is capable of preventing the polysilicon layer from reacting with the contact structure.

47. The memory cell of claim 46, wherein the insulating structure is in contact with the polysilicon layer, the tungsten nitride layer, and the platinum-ruthenium layer.

48. The memory cell of claim 46, wherein platinum-ruthenium layer is separated from the polysilicon layer by the insulating structure.

49. A memory cell comprising:

a capacitor;

a transistor;

a contact structure coupling the capacitor to the transistor; and

an insulating structure encircling the contact structure.

50. The memory cell of claim 49, wherein the insulating structure is located between the contact and a borophosphosilicate glass layer.

51. The memory cell of claim 49, wherein the insulating structure is fabricated from tungsten nitride.

52. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field effect transistor (MOSFET);

a contact coupling the capacitor to the MOSFET; and

an oxide structure encircling the contact.

53. The memory cell of claim 52, wherein the oxide structure is in contact with a polysilicon layer.

54. The memory cell of claim 52, wherein an air gap separates the oxide structure from a polysilicon layer.

55. A memory cell comprising:

a capacitor;

a transistor;

a contact structure including a polysilicon layer, a tungsten nitride layer, and a ruthenium silicide layer, the contact structure coupling the capacitor to the transistor; and

an insulating structure encircling the contact structure.

56. The memory cell of claim 55, wherein the transistor is a bipolar transistor.

57. The memory cell of claim 55, wherein the insulating layer is separated from the polysilicon layer by an air gap.

58. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field effect transistor (MOSFET);

a contact structure including a polysilicon layer, a tungsten nitride layer, and

a platinum-ruthenium layer, the contact structure coupling the capacitor to the MOSFET; and

an insulating structure encircling the contact structure.

59. The memory cell of claim 58, wherein the insulating structure is in contact with the contact structure.

60. The memory cell of claim 58, wherein the insulating structure is in contact with the platinum-ruthenium layer.

61. A system comprising:

a processor; and

one or more memory cells coupled to the processor, wherein at least one of the memory cells includes a contact having an insulating structure capable of preventing a conductive layer from interacting with a barrier layer.

62. The system of claim 61, wherein the processor is a microprocessor.

63. The system of claim 61, wherein at least one of the memory cells is a dynamic random access memory (DRAM) cell.

64. A system comprising:

a processor; and

one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact having an insulating structure capable of preventing interaction between a polysilicon layer and a barrier layer.

65. The system of claim 64, wherein the processor is a reduced instruction set (RISC) processor.

66. The system of claim 64, wherein the barrier layer prevents migration of oxygen atoms into a substrate.

67. A system comprising:

a processor; and

one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact structure including a barrier structure fabricated from silicon nitride.

68. The system of claim 67, wherein the barrier structure encircles the contact structure.

69. The system of claim 67, wherein the contact structure includes one or more barrier layers.

70. A system comprising:

a processor; and

one or more memory cells, wherein at least one of the memory cells includes a contact structure having an insulating structure encircling the contact structure.

71. The system of claim 70, wherein the contact structure includes a polysilicon layer and two barrier layers.

72. The system of claim 70, wherein the contact structure includes a barrier layer capable of blocking migration of silicon atoms and a barrier layer capable of blocking migration of oxygen atoms.

73. A system comprising:

a processor; and

one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact having a polysilicon layer, a tungsten nitride layer, and a ruthenium layer.

74. The system of claim 73, wherein the polysilicon layer is isolated from the ruthenium layer.

75. The system of claim 73, wherein the tungsten nitride layer is adjacent to the ruthenium layer.

76. A system comprising:

a processor; and

one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact structure having a tungsten nitride layer, a ruthenium silicide layer, and an air gap encircling the tungsten nitride layer.

77. The system of claim 76, further comprising:

an oxide layer encircling the contact structure.

78. The system of claim 77, wherein the ruthenium silicide layer is in contact with the oxide layer.

79. A method comprising:

forming an active device on a substrate;

forming a passive device on the substrate; and

forming a contact structure including a barrier structure for coupling the passive device to the active device.

80. A method comprising:

forming a metal-oxide semiconductor field-effect transistor (MOSFET);

forming a passive device; and

forming a contact structure including a barrier structure capable of coupling the passive device to the MOSFET.

81. A method comprising:

forming a conductive layer on a base structure having a surface;

forming a first barrier layer above the conductive layer;

etching the conductive layer and the first barrier layer to a level below the surface;

forming a barrier structure that encircles the conductive layer and the first barrier layer;

forming a second barrier layer above the first barrier layer; and

polishing the second barrier layer and the surface.

82. The method of claim 81, further comprising:

forming an active device below the conductive layer.

83. The method of claim 82, further comprising:

forming a passive device above the second barrier layer.

84. A method comprising:

forming a polysilicon layer on a base structure having a surface;

forming a tungsten nitride layer above the conductive layer;

etching the polysilicon layer and the tungsten nitride layer to a level below the surface;

forming a silicon nitride structure that encircles the polysilicon layer and the tungsten nitride layer;

forming a ruthenium silicide layer above the first barrier layer; and

polishing the ruthenium silicide layer and the surface.

85. The method of claim 84, further comprising:

forming a MOSFET below the conductive layer.

86. The method of claim 85, further comprising:

forming a capacitor above the second barrier layer.

87. A method comprising:

forming a conductive layer on a base structure having a surface;

forming a first barrier layer above the conductive layer;

forming a second barrier layer above the first barrier layer;

etching the first barrier layer and the second barrier layer;

etching the conductive layer and the first barrier layer to a level below the surface;

forming an oxide layer above the second barrier layer; and

removing the oxide layer from above the second barrier layer.

88. The method of claim 87, further comprising:

forming a transistor below the conductive layer.

89. The method of claim 88, further comprising:

forming a passive device above the second barrier layer.

90. A method comprising:

forming a polysilicon layer on a base structure having a surface;

forming a tungsten nitride layer above the conductive layer;

forming a ruthenium silicide layer above the tungsten nitride layer;

etching the tungsten nitride layer and the ruthenium silicide layer;

etching the polysilicon layer and the tungsten nitride layer to a level below the surface;

forming an oxide layer above the ruthenium silicide layer; and

removing the oxide layer from above the ruthenium silicide layer.

91. The method of claim 90, further comprising:

forming an active device below the conductive layer.

92. The method of claim 91, further comprising:

forming a capacitor above the second barrier layer.

93. A method of forming a contact, the method comprising:

forming a structure having a plug volume above a substrate;

forming a polysilicon layer in the plug volume;

forming one or more barrier layers above the polysilicon layer;

etching an outer perimeter to recess the outer perimeter of the plug volume down to a tungsten nitride layer;

forming a barrier structure in the outer perimeter;

etching the barrier structure to leave a sidewall above the tungsten nitride, but still expose the top surface;

depositing the oxygen barrier layer to fill the rest of the plug; and

polishing to isolate individual plug features.

Abstract

This invention relates to contact structures for use in integrated circuits and methods of fabricating contact structures. In one embodiment, a contact structure includes a conductive layer, one or more barrier layers formed above the conductive layer, and a barrier structure encircling the polysilicon layer and the one or more barrier layers. In an alternate embodiment, a contact structure is fabricated by forming a polysilicon layer on a substrate, forming a tungsten nitride layer above the polysilicon layer, and etching the polysilicon layer and the tungsten nitride layer to a level below the surface of a substrate structure. A silicon nitride layer is formed above the tungsten nitride layer, and a ruthenium silicide layer is formed above the silicon nitride layer. The ruthenium silicide layer is then polished.

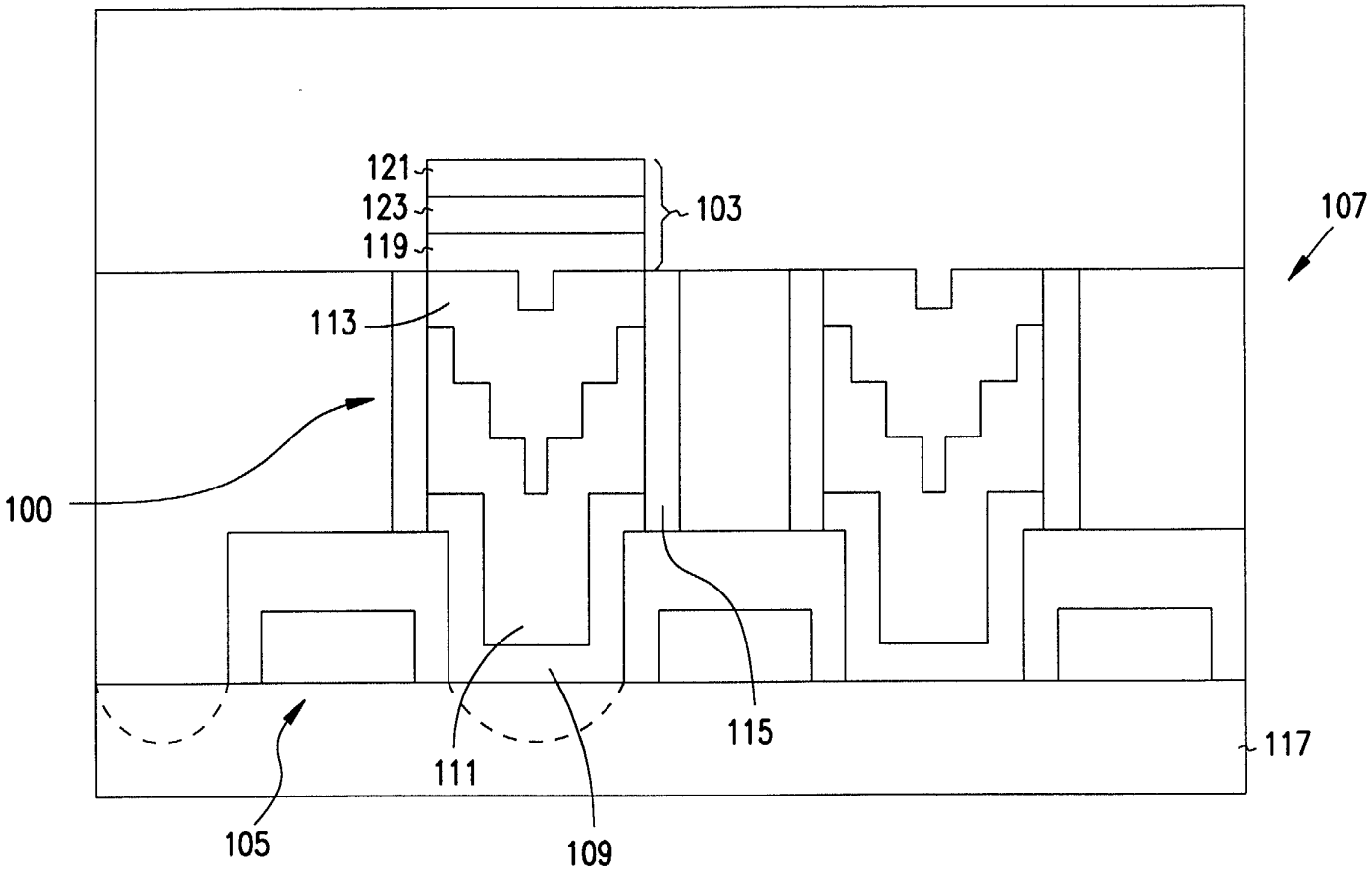


Figure 1

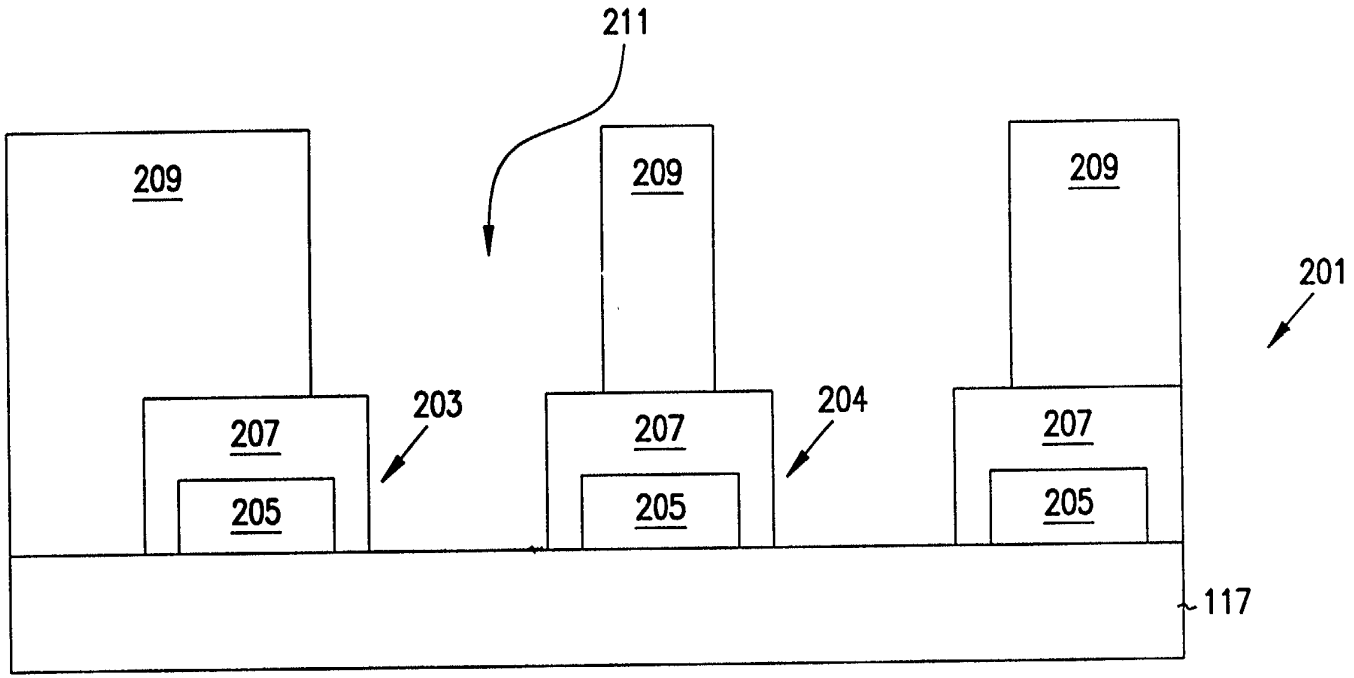


Figure 2

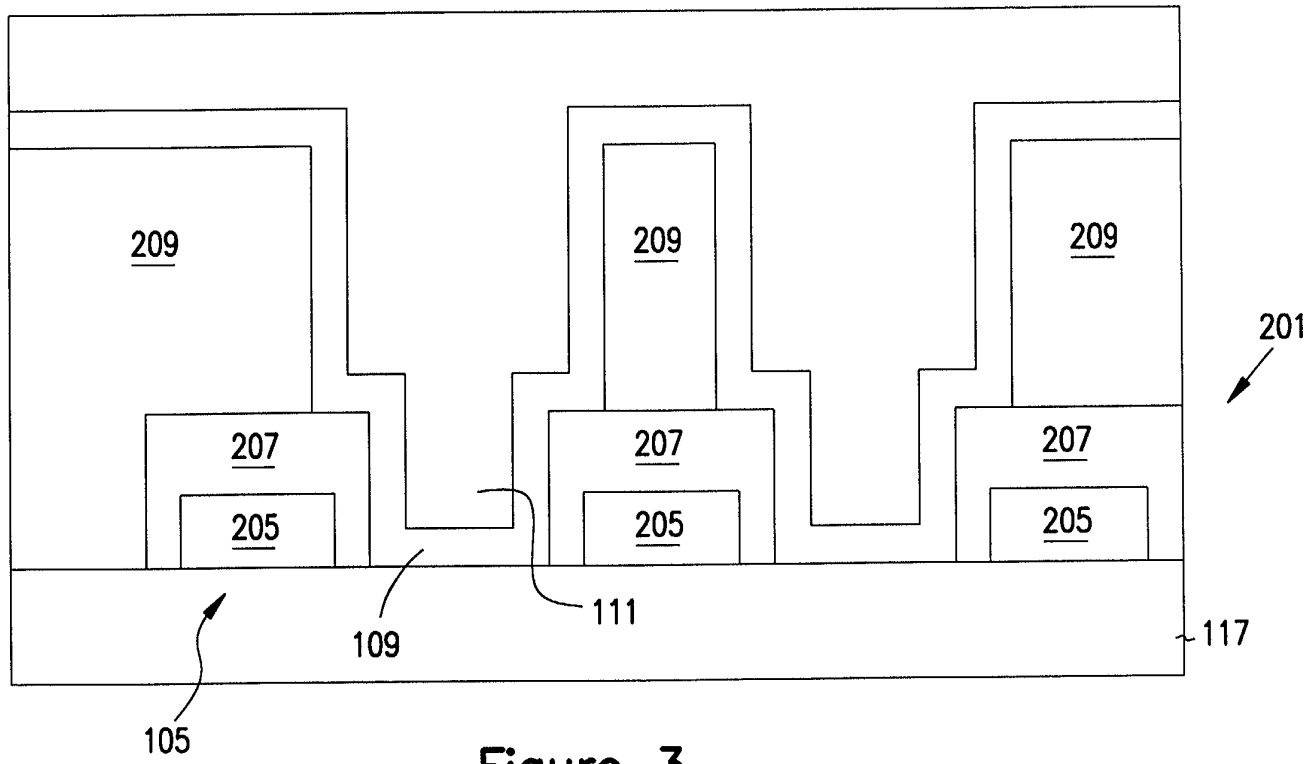


Figure 3

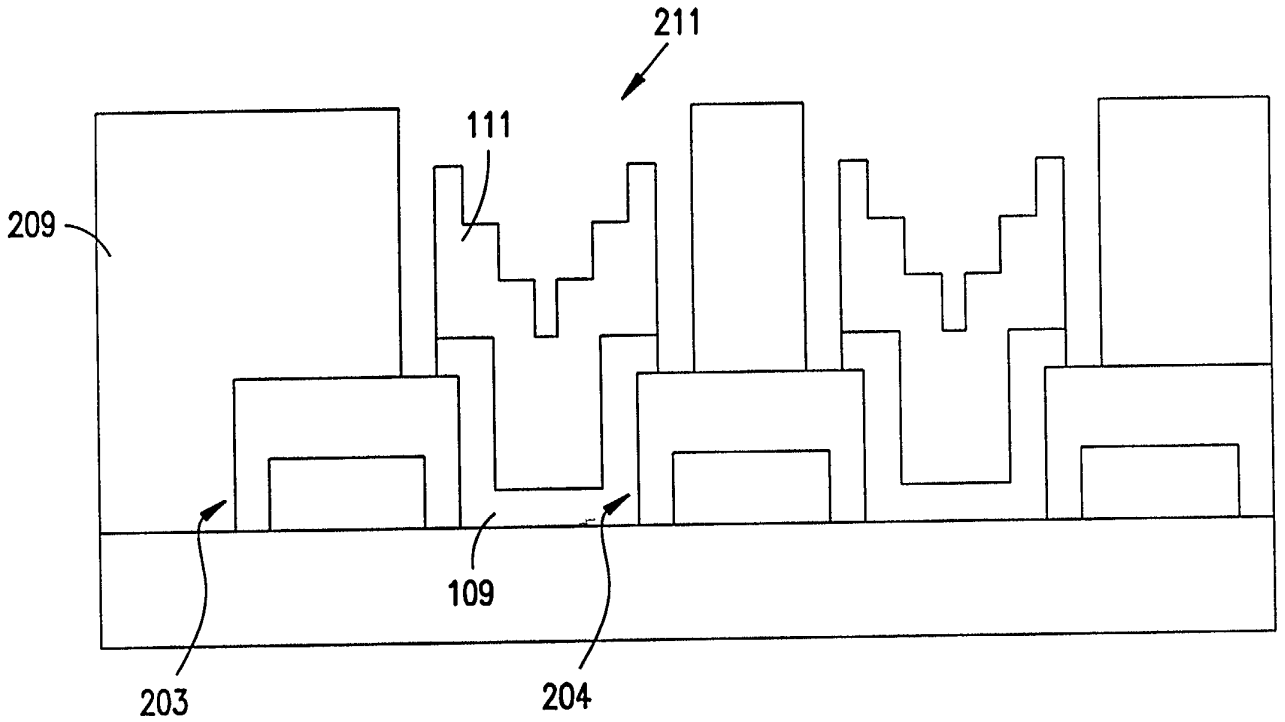
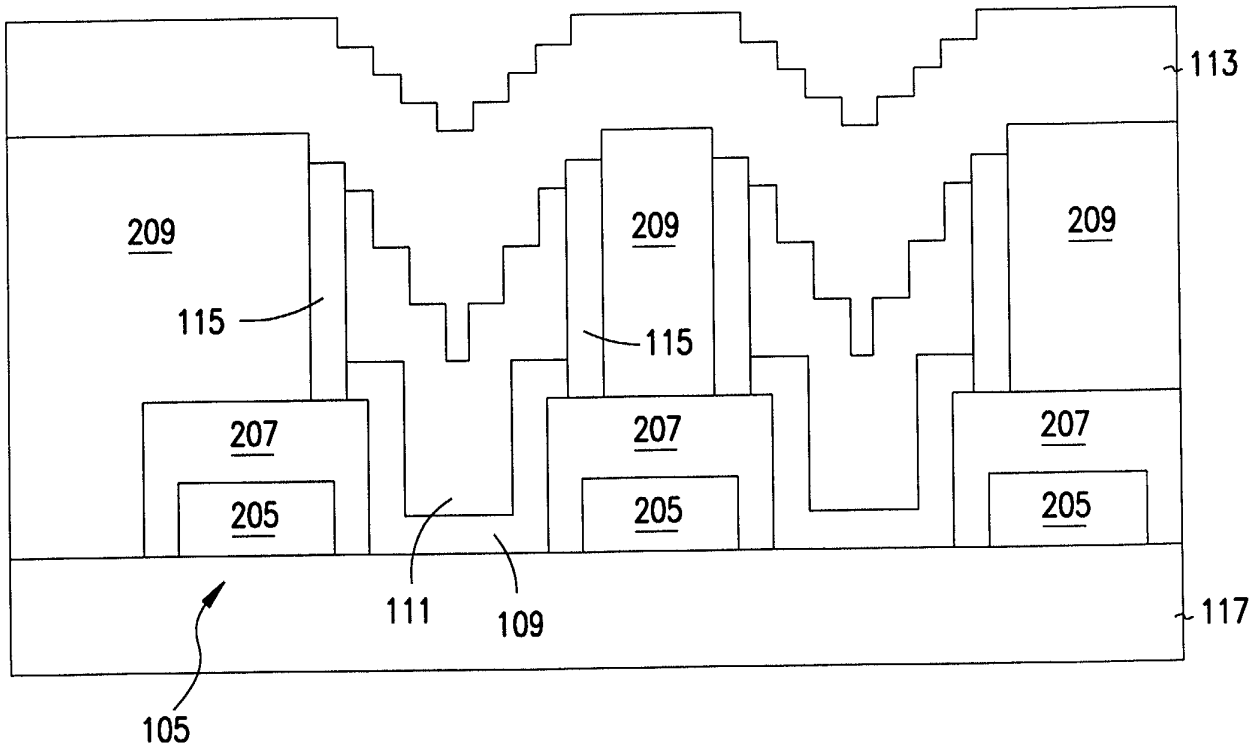


Figure 4



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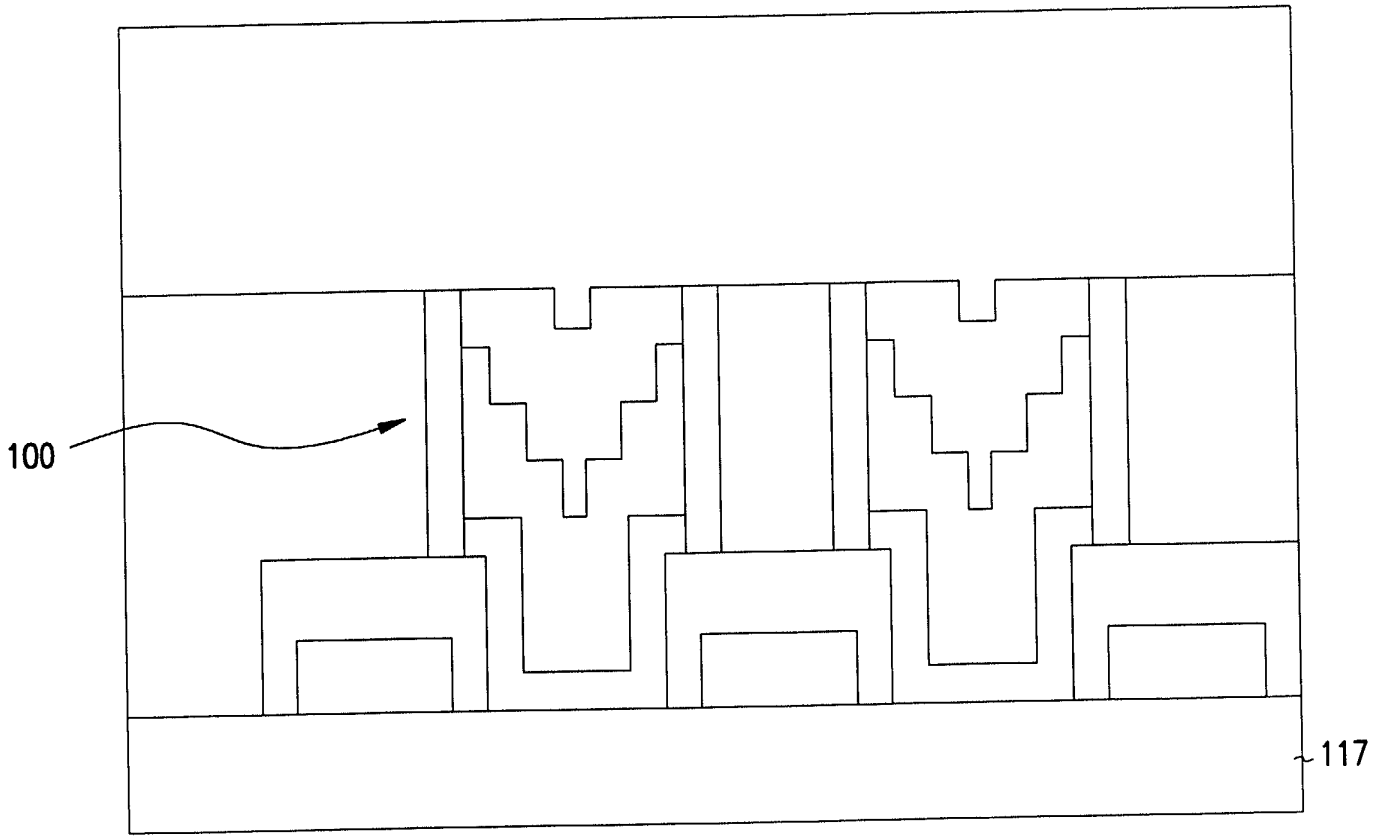

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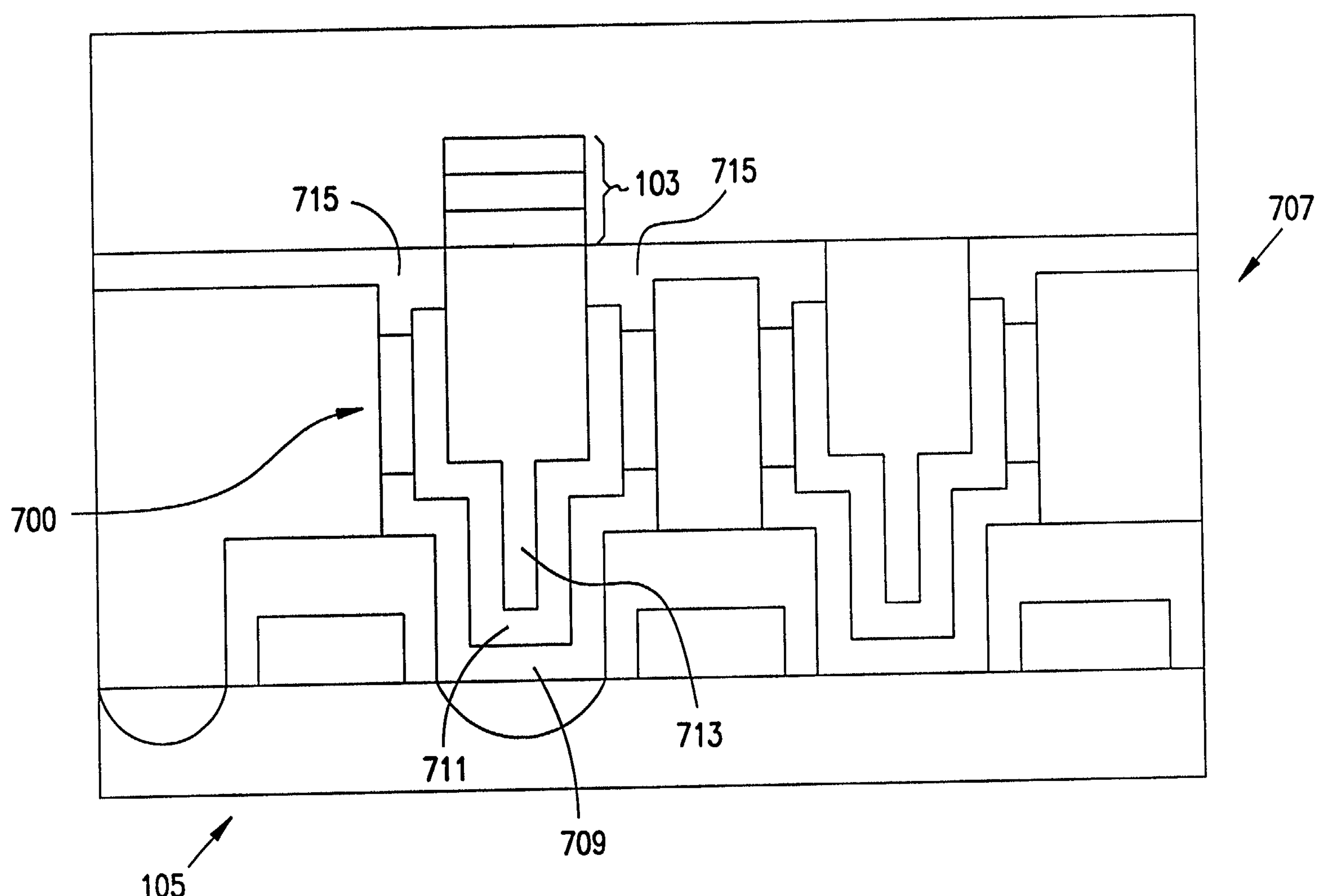

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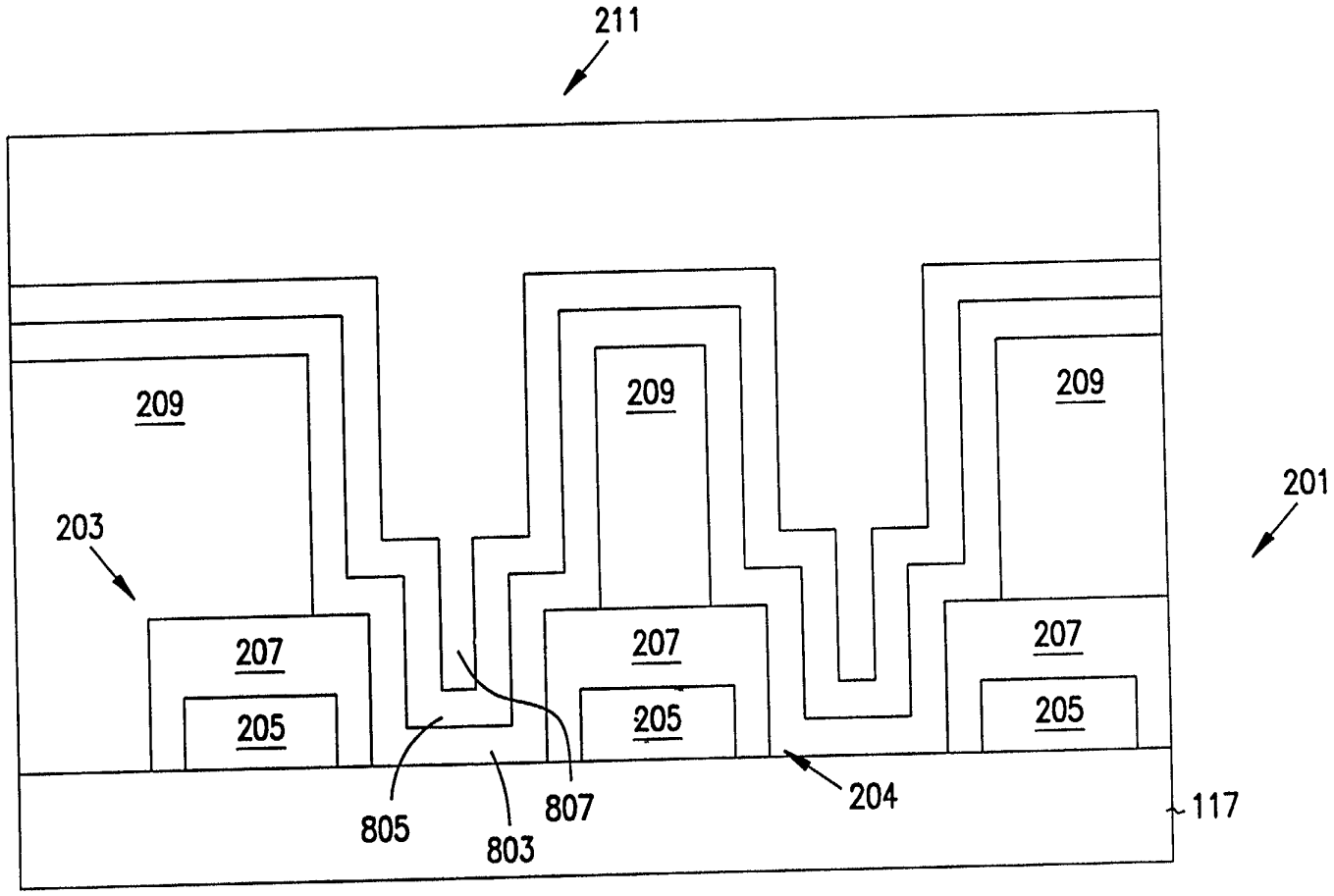

Figure 8

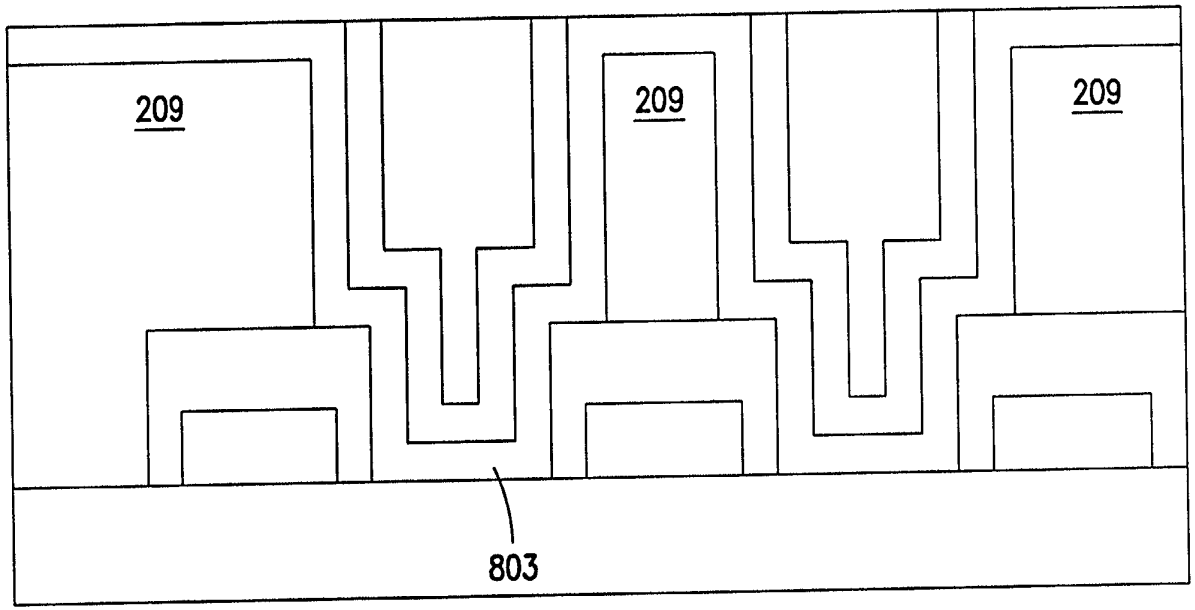

Figure 9

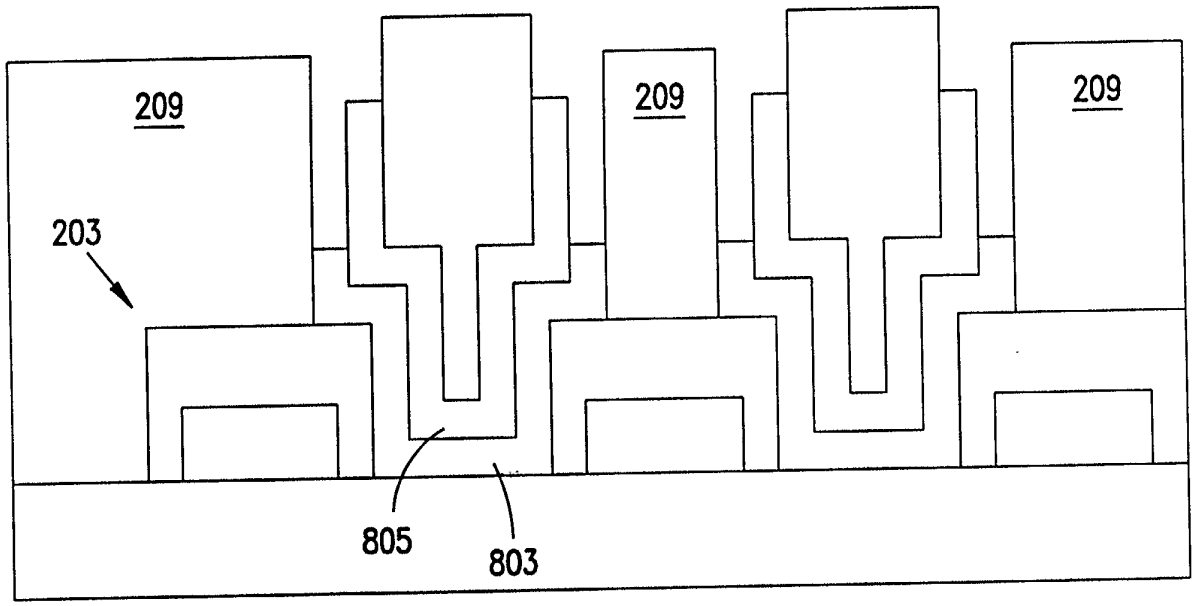

Figure 10

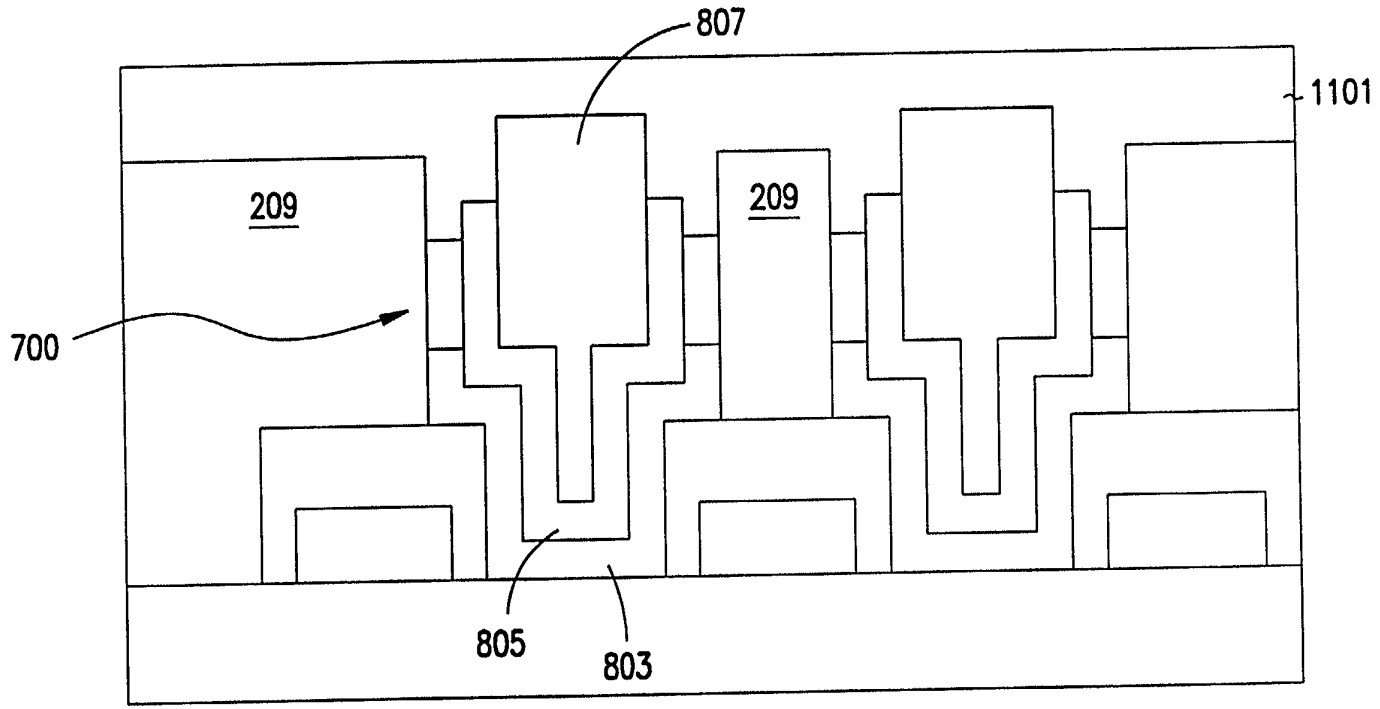

Figure 11

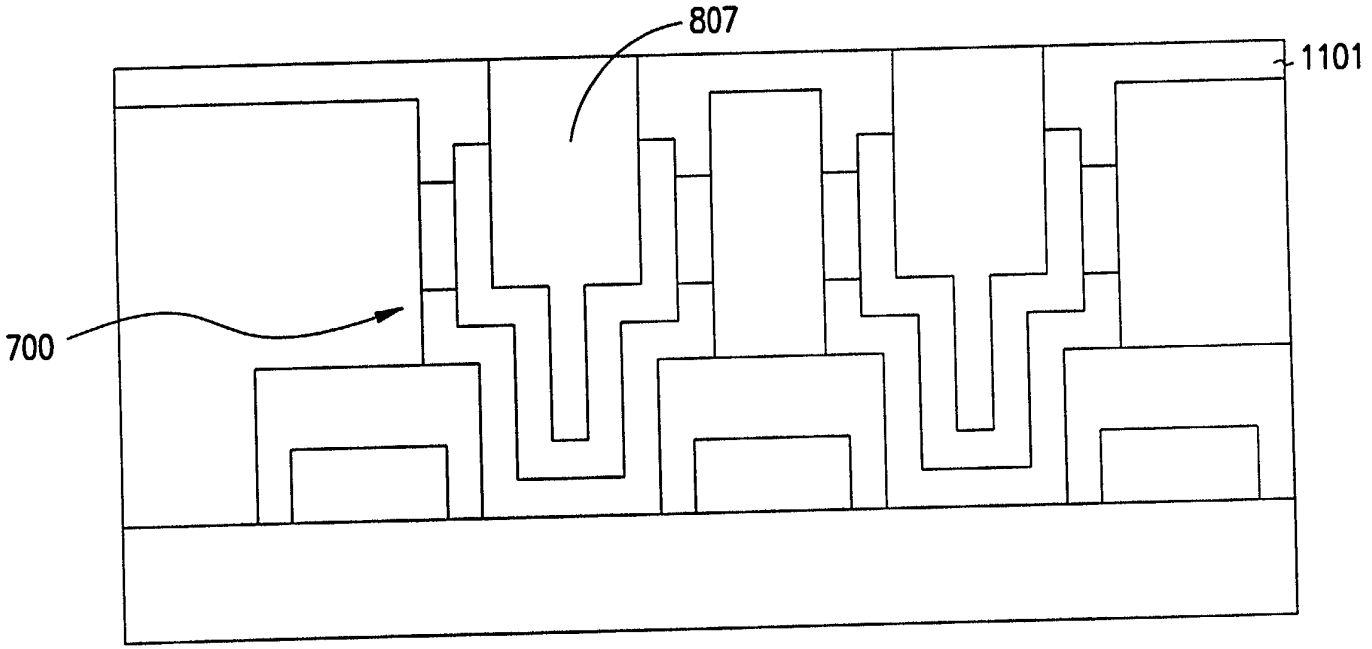

Figure 12

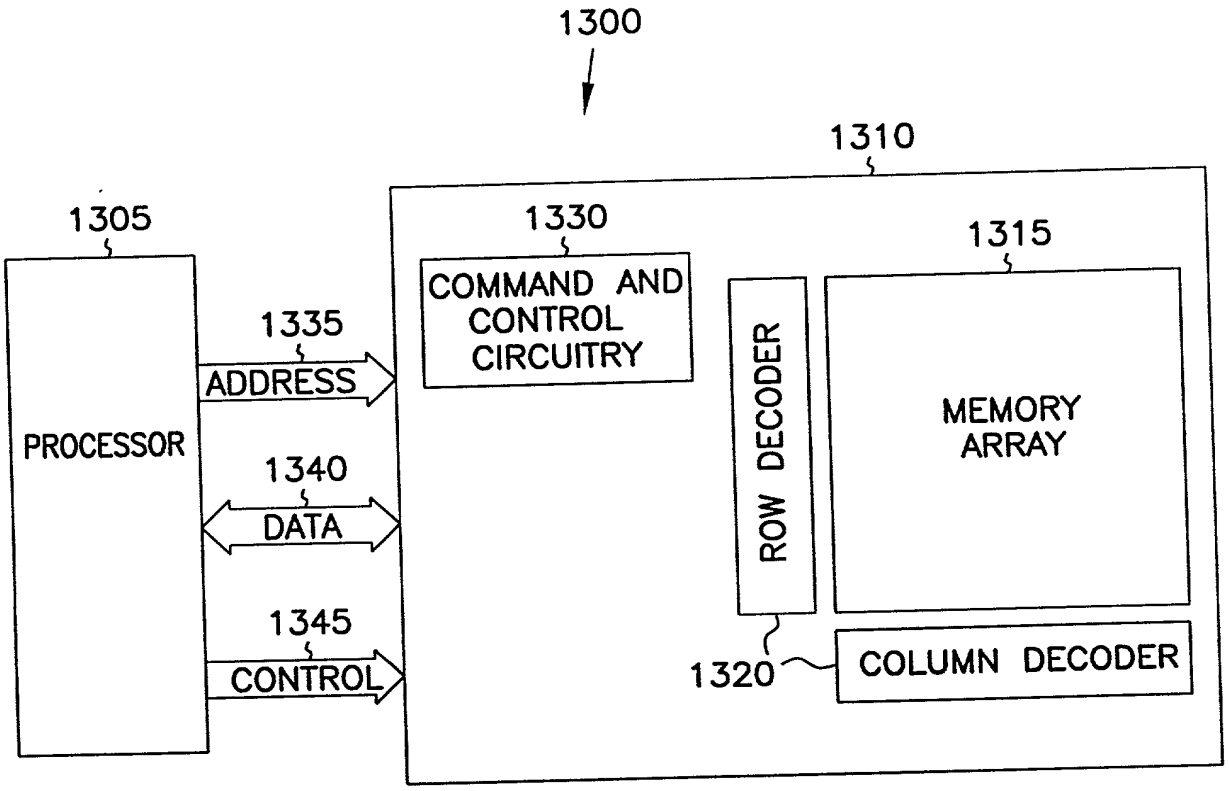
1300
1310
1305
1330
1315
COMMAND AND CONTROL CIRCUITRY
ROW DECODER
MEMORY ARRAY
1335
ADDRESS
PROCESSOR
1340
DATA
1345
CONTROL
1320
COLUMN DECODER

Figure 13

SCHWEGMAN ■ LUNDBERG ■ WOESSNER ■ KLUTH

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **CONTACT STRUCTURE**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

No such claim for priority is being made at this time.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

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Forrest, Bradley A.	Reg. No. 30,837	McCrackin, Ann M.	Reg. No. 42,858	Tong, Viet V.	Reg. No. 45,416
Gamon, Owen J.	Reg. No. 36,143	Moore, Charles L., Jr.	Reg. No. 33,742	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	Nama, Kash	Reg. No. 44,255	Woessner, Warren D.	Reg. No. 30,440
Huebsch, Joseph C.	Reg. No. 42,673	Nelson, Albin J.	Reg. No. 28,650		

☐ I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to **Schwegman, Lundberg, Woessner & Kluth, P.A.** at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402
Telephone No. (612)373-6900

☐ I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Fred Fishburn**
Citizenship: **United States of America** Residence: **Boise, ID**
Post Office Address: 1213 Harrison Blvd.
Boise, ID 83702

Signature: _____ Date: _____
Fred Fishburn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.